MARKED-UP AMENDMENTS

**In The Specification**

Please amend the specification as follows.

In the paragraph beginning at page 12, line 8

-- This issue can also be solved by the invention. [Since the bonding pad of the invention include a top metal layer 250 of Fig. 4 and] By means of the stacked metal layer 208, [. The] the bonding pad opening 270 can be [adjusted] placed [at the location] right above the device region. As a result, [the available] more substrate surface can be [more efficiently] favorably available [used]. --

In the paragraph beginning at page 12, line 15

-- Referring to Fig. 23, a device 32, such as a field effect transistor, is formed on a substrate 30. Metal layers 51, 52, 53, 54, 55 and 56 are formed in a dielectric layer 60 over the device 32, in which the dielectric layer 60 serves as an isolation and a frame to stack the metal layers 51, 52, 53, 54, 55, 56. The dielectric layer 60 [can also] may further include several sub-layers to hold and isolate the metal layers. A bonding pad includes the metal layers 55 and 56 and is covered by [the] a passivation layer 80. The passivation layer 80 includes a bonding pad opening 82[,] which exposes a portion of the metal layer 56. The metal layers 51 and 52 near the substrate 30 [are used to] serve as, for example, signal lines electrically connected to the substrate 30 by means of via plug 70, and the metal layers 53 and 54 are designed to be planar layers and [used to] serve as, for example, power lines. [A] The passivation layer 80 is formed on [a] the dielectric layer 60, and the bonding pad opening 82 is formed in the passivation layer 80 to



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expose the metal layer 56. A bonding wire 84 is attached to the metal layer 56 within the bonding pad opening 84. Each pair of the metal layers 51, 52, 53, 54, 55 and 56 is isolated by the dielectric layer 60. The metal layers 55, 56 are coupled by a via plug 75 and the metal layers 51, 52 are coupled by a via plug 71. The metal layers 52, 53 and 54 serving as signal lines and power lines are also coupled by via plugs (not shown)[, and] as well as the metal layers 54 and 55 [are similar]. However, theses via plugs should not be formed under the bonding pad opening 82. Thus, the metal layers 53, 54 can be used [to be the] as buffer layers, and the bonding stress [borne] on the active devices can be reduced through these buffer layers. --

**In The Claims**

Please amend the claims as follows.

26. (Once amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one [and other] another by a plurality of via plugs in the dielectric layers, the via plugs being placed in alternating manner with respect to one another through the stack;

an uppermost metal layer positioned on the stack and electrically connected to the stack, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

a passivation layer having a bonding pad opening positioned on the uppermost metal layer for externally electric connection.



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28. (Once amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one [and other] another by a plurality of via plugs [in] through the dielectric layers and are placed in a concentric circle arrangement;

an uppermost metal layer positioned on the stack and electrically connected to the stack; and

a passivation layer having a bonding pad opening on the uppermost metal layer for externally electric connection.

30. (Once amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; and

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad being aligned with the doped region.

36. (Once amended) A semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; [and]



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a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad is aligned with the doped region, and wherein the metal layers in the stack are in a concentric circle arrangement; and

a device under the bonding pad.

39. (Once amended) A semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; [and]

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by means of a plurality of via plugs, wherein the bonding pad is aligned with the doped region; and wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

a device under the bonding pad.



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